

STILL VIDEO CAMERA PROVIDED WITH REMOVABLE RECORDING MEDIUM

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EC Classification:
Equivalents:

Abstract

PURPOSE: To improve the operability by transferring and recording a recorded picture to a removable 2nd picture recording medium from a camera.

CONSTITUTION: Whether or not an IC card 41 is loaded to a camera is discriminated and when the IC card is loaded to the camera, the state of a memory of the IC card 41 is inputted from a signal processing CPU 51 and a signal CSDP is brought into logical H to make the communication complete. When the IC card is not recorded and the internal memory has a recorded picture, and when the processing of all picture data recorded in the internal memory is finished, number of frames stored in the internal memory 40 is subtracted from number of frames able to be recorded on the IC card 41 and the resulting frame number is displayed for the recordable frame number onto the IC card 41 to make the processing complete.

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り、創作性の点で著しく不便であった。
この説明は上記問題を解決することを目的とするものである。

一級中のなほりすを断り取置

この説明は上記問題を解決するため、内部メ
モリに格納された画像データを１カードごとに取り出
すに必要に、記憶媒体に転送記録を要するようにしたもので
あって、複製機分の画像記録領域を備え、カメラ
装置に格納された第１の画像記録媒体と、複製機
装置に格納された第２の画像記録媒体とを備えたス
キャンタイプカメラにおいて、前記第１の画像記録
媒体のカメラ本体への複製動作を演出する演出手
段と、前記演出手段により前記第２の画像記録
媒体が、前記カメラ本体に複製されていることが検出され
たと、前記第１の画像記録媒体に記録されてい
る画像データを前記第２の画像記録媒体の記録可能
領域に複製せよと前記手段を制御手段に指示することとを
要する。

(附)

カメラ本体とフラッシュ装置の性能用点である。次に操作スイッチについて説明する。S3はカメラの望遠・近接切替スイッチで、遠近切替スイッチである。

○ＦＦ：カメラの起動が禁止される。

メ
RBC: 記録モードであつて、カメラの内蔵メ
モリ、あるいは着脱自在な外部記憶媒体
(以下、ICカードという)に画像が記録
される。

PLAYY 両生モードであって、内蔵メモリにあるいはICカードに記録されている画像が再生され、映像信号が出力される。この信号に基づいて図示しないビデオ表示装置に記録画像が再生される。

ERASE-ALL: 内部メモリとICカードに記憶されている画像を全て消去する消去モードである。

ERASE-SINGL:内題メソリあるいは
ICカードに記憶されている複写面盤1枚

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○取組の名目
事業目在が肥後県を模えたスチルビデオカメラ

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1981

一、 衆議院の決議は、衆議院の議決を経て、内閣に送付され、内閣は、衆議院の決議を執行する。衆議院の決議は、衆議院の議決を経て、内閣に送付され、内閣は、衆議院の決議を執行する。

「日本の未来は」

[illegible]

また、オールド・ファッション・カードなどの記録は本館の所蔵にない。代わりの資料を入手し、カードなどの記録は本館に保存されなければならない。図鑑記録が可能なものは保存される。また、オールド・ファッション・カードなどの記録は本館の所蔵にない。代わりの資料を入手し、カードなどの記録は本館に保存されなければならない。図鑑記録が可能なものは保存される。

「希望が実現しようとする問題」

[illegible]

- 649 -

-650-

リセットスライツ³がERASE (SINGL. ALL) といった位置であつてもよい) 位置にあるとONされる。その場合動作が実行され、プロセッサスライツ56がPHUT位置にあるとONされる。また、MANUAL、即ち手動に設定すると、アクセススライツ54、55の操作により1割ずつ増進される。

59はマクロ制御用スライツ、510はフラッシュメモリを設定するスライツである。512は日付設定用モードスライツで、ONとする時に、Y (年) - M (月) - D (日) - H (時) - M1 (分) - Y (年) の順に順次的にモードが切替えられる。513は日付設定スライツで、スライツ512

で選択されたモードのデータブロック図を示す。第2図はカメラの新撮回路のブロック図を示す。

30はカメラ本体を制御するCPU、31は撮写制御部であつて、撮写制御の制御再生処理を行う。その制御は、32はCCDなどからなる撮写制御部(以下CCDという)で、撮写レンズ2から入射した画像を撮写制御部に送付する。33は撮写CCDから出力された撮写制御部の制御二重サンプリング部、34は撮写制御部をデジタ化信号に変換するA/D変換部、35はCCD 32、サンプリング部33、A/D変換部34の同期をとるクロック発生回路で、CPU30から出力される同期信号INREL、EXSTPで制御される。36は撮写回路で、撮写制御部を制御し、撮写制御部をCPU30に出力すると共に、撮写回路として動作し、フラッシュの撮写制御を行う。37はフラッシュ制御部で、撮写制御部とコンデンサを備えている。38は撮写部、CPU30から出力される同期信号INREL、EXSTPで制御される。

次に撮写部で伝送される信号について説明する。CHSTAはフラッシュ制御部37のコンデンサに充電制御を指示する信号、CHCはフラッシュ制御部37のコンデンサ充電完了を示す信号、FLSTAはフラッシュ制御部37に対してフラッシュ撮写を指示する信号、FSTOPは撮写回路36で送出したフラッシュの光量が所定値に達したと8 (撮写完了時) にフラッシュの撮写停止を指示する信号である。

INRELはシャッタレリーズ開始信号で、CPU30からクロック発生回路35に出力される。クロック発生回路35はこの信号に反応して撮写制御部の動作を指示する信号EXSTAをCPU30に出力する。EXSTPは撮写回路36に出力する。CPU30からクロック発生回路35に出力される。また、シャッタレリーズ開始信号INREL及び撮写回路終了信号EXSTPは撮写制御部31にも出力される。

CSDPはCPU30と信号処理部31との間

の信号の伝送を制御する信号、SOUT、SINはCPU30と信号処理部31との間でシリアルデータとして伝送されるデータ信号、SCKはCPU30から信号処理部31に伝送されるシリアルクロック信号、BUSYは信号処理部31が信号処理中であることをCPU30に伝える信号、LBCはマクロ制御が実行されることを示す信号、VOUTは信号処理部31から出力される撮写信号である。

第3図は信号処理部31の構成を示すブロック図である。31は信号処理部31全体の制御を行う信号処理CPU、52は撮写制御部の制御(圧縮を含む)を行う信号処理回路、53はクロック発生回路35からのクロック信号を受けてアドレス信号を発生するアドレス発生回路である。

54は信号処理回路52から出力される信号RD/CDに基づいて、アドレス発生回路53から出力されるアドレス信号、即ちCD32から出力される撮写制御部マクロメモリ55に記録する際に使用するアドレス信号バスと信号処理部

を示す。

第5図はフラッシュ制御部の回路図を示す。この回路は撮写の回路である。その構成と動作の原理について説明する。図において61は撮写制御部、62はDC/DCコンバータからなる昇圧回路、63は電圧制御用主コンデンサ、64はオシレータ、65はトリガ回路、66はキャパシタ、67はタイミスタを示す。

次に、その動作について説明すると、カメラのCPU30から信号L1に印加されている充電制御信号CHSTAが"H"になると、昇圧回路62が動作を開始して、電圧61の電圧が上昇され、主コンデンサ63に充電される。主コンデンサ63の満ち電圧が所定値に達すると、信号L3に出力される信号CHCが"H"となり、CPU30に充電完了を知らせる。カメラのCPU30から信号L4に印加されているフラッシュの動作を指示する信号FLSTAが"H"になると、トリガ回路66が動作し、キャパシタ66の電圧を制御する。カメラの動作回路

以下のとおりである。一般に撮影レンズを用いて無限遠にある物体の像を結像させる場合、撮影レンズの軸方向位置に起因して被写体は撮影レンズと同心の球面となる。したがって撮影レンズにおいては軸上と軸外の両方の位置で同等の像を得ることになり、軸上で被写体と被写体正を達成できれば、軸外の位置も満足される。したがって、普通のレンズ系に比較して小型で単純な光学系であるにもあわらず、遠近両方写正を確保せば、周辺光量の下がりが少なく、明るい結像性能の高いレンズを得ることが出来るのである。

次に、CPU30で実行されるカメラの制御動作を第7図から第17図に示すフローチャートを参照して説明する。

第7図は制御全体の動作を示すフローチャートで、各種スイッチ類の状態を調べ、スイッチに対して応じた処理ルーチンへ移ることを示している。制御動作の開始と共に、まずモード切換スイッチS3がOFFの位置に設定されているか否かを調べ、OFFの場合はモード切換ルーチンへ移る

ONであれば表示をOFFとする(ステップP134、P138)。ICカード41がカメラ本体に挿入されていることを検出表示がONか否かを判定し、ONであれば表示をOFFとする(ステップP137)。日付表示をOFFとし、記録面の状態を示すカウンタ表示をOFFとし(ステップP138、P139)、電源38に対して番号PWCを“H”として電源状態を診断し(ステップP140)、主ルーチンに戻る。

第8図は第7図に示すフローチャートのステップ103として示したモード切換スイッチS3が記録モード(REC)の場合の処理モードルーチンを示す。まず、モード切換スイッチS3がOFFからRECの位置へ切換ったか否かを判定し(ステップP151)、切換った場合は番号PWCを“L”として電源38をONとする(ステップP152)。ICカード41がカメラに挿入されているか否かを判定し(ステップP153)、挿入されている場合は、ICカード表示をONとし(ステップP154)、番号

CSDPを“L”として番号表示CPU51からICカード41の記録状態(記録可能など)を表示するモード切換を受け、交換終了後番号CSDPを“H”として交換を終了する(ステップP155、P156、P157)。ICカード41の記録面が一ばいで記録不可か否かを判定し(ステップP158)、記録不可の場合は終了の表示をONとし、記録可能状態を示すカウンタ表示をONとし、日付表示をONとして(ステップP160、P161、P162)、主ルーチンに戻る。ステップP158の判定でICカードに記録可能があり、記録可能な場合はステップP160は省かれる。

ステップP153の判定でICカード41が挿入されていないと判定されたときは、番号CSDPを“L”として番号表示CPU51から内部メモリ40の記録状態(記録可能など)を表示するモード切換を受け、交換終了後番号CSDPを“H”として交換を終了して(ステップP165、P166、P167)、ステップ

(ステップP100、P101)。モード切換スイッチS3がREC、即ち記録モードに設定されているか否かを調べ、記録モードの場合は記録モード処理のルーチンへ移る(ステップP102、P103)。シャッターリリースボタンでONするスイッチS1の位置を調べ、ONの場合はS1 ON処理ルーチンへ移る(ステップP104、P105)。モード切換スイッチS3がPLAY、即ち再生モードに設定されているか否かを調べ、再生モードの場合は再生モード処理のルーチンへ移る(ステップP106、P107)。モード切換スイッチS3がERASE、即ち消去モードに設定されているか否かを調べ、消去モードの場合は消去モード処理のルーチンへ移る(ステップP108、P109)。アクセススイッチS4(UP)の状態を調べ、ONされているときはS4処理ルーチンへ移る(ステップP110、P111)。アクセススイッチS5(DOWN)の状態を調べ、ONされているときはS5処理ルーチンへ移る

P161に移る。

ステップP161の判定でOFFからRECに切換ったのでなければ、モード切換スイッチS3がPLAYからRECの位置へ切換ったか否かを判定し(ステップP170)、切換った場合は番号PWCを“L”として番号表示CPU51、番号CSDPを“L”として番号表示CPU51からRECに切換ったことを知らせる番号を出し、番号CSDPを“H”として交換を終了して(ステップP171、P172、P173、P174)、主ルーチンに戻る。

第10図(a)乃至第10図(f)は第7図に示すフローチャートのステップP105として示したリリースボタンの第1段階でONするスイッチS1がONとされた場合の処理ルーチンである。まず、記録モード(REC)が否かを判定する(ステップP201)。記録モードでないときは撮影が不可能であることを示すから、ステップP210以降の処理に移る。まず、マクロ撮影スイッチS9がONか否かを判定し、ONの場合はマクロ撮影ランプLAを点灯する(ステップP210、P211)。マクロ撮影でない場合はステップP211は省かれる。闪光灯36で閃光した被写体深度をA/D変換して入力する(ステップP212)。マクロ撮影スイッチS9がONか否かを判定し(ステップ

P208)。

ステップP201の判定で記録モードの場合、記録面の状態表示カウンタが0か否かを判定し(ステップP202)。0の場合はこれ以上画像記録が不可能なことを示すから、タイマ1に所定値K1をセットして計時を開始させ、カウンタ表示を点滅させる(ステップP203、P204)。タイマ1の計時終了を待ち、カウンタ表示を連続点灯で切換え(ステップP205、P206)、主ルーチンに戻る。

ステップP202の判定でカウンタが0でない場合は、即ち撮影が可能であることを示すから、ステップP210以降の処理に移る。まず、マクロ撮影スイッチS9がONか否かを判定し、ONの場合はマクロ撮影ランプLAを点灯する(ステップP210、P211)。マクロ撮影でない場合はステップP211は省かれる。闪光灯36で閃光した被写体深度をA/D変換して入力する(ステップP212)。マクロ撮影スイッチS9がONか否かを判定し(ステップ

S4. あらうはS5OFFP65ONに化した
て、否かを判する（ステップ623一
624）。タイ4の計算が完了した場合
は、ステップ605に戻り、再度タイ4によ
る計算を始めて次の図面の処理に移る。または
タイ4の計算が完了前にスイ5、タイ4の計算を終
了したのになった場合は、タイ4の計算を停
止し、再度図面のプロットデータを算出す（ス
テップ653、626）。

同装置のプロットテープを取出し、プロット/照像動作スイッチS8の操作によるプロットテープの記録及び解除を行うスイッチP628～P639の配線は、アグニスタイプ54の図面におけるスイッチP419～P432の配線と同一装置であるから、ここでは説明を省略する。

スチッP604の判定でアクセススチッ
S6がOPPからONに変化した場合は、スチッ
P6041に替る。まず、タイマ4に所定値K4

[illegible]

第17図は第14図に於けるプロチャートのス
チャートP119とて示した日付位置調整のフ
ローチャートである。まず、日付位置スィッチ
S130Nを閉することにより「月」位置モードと
なり、アクタススィッチS4、S5の操作で所望
の月を設定する(スチャートP701)。モードシ
フトスィッチS12をONにすると「月」位置
モードに切り、スィッチS4、S5の操作で所
望の月を設定する(スチャートP702。
P703)。以下、同様にモードP702、S5の
スィッチS12をOFFにするとモードP703、S5の

から入力し、標準CSDPを“N”として文通を終了する(スチップP802→P804)。ICカードは記憶済み、または内蔵メモリに記憶データが書きこばれ(スチップP805、P806)、ICカードが戻され、内蔵メモリに記憶済みである場合はスチップP807に移る。ICカードが記憶済みでない限り、内蔵メモリ、ICカードは消去され、メモリはリセットされる。

内部メモリの記憶面番の先頭の桁番号をX（この実施例では10）とし、ICカードに記憶可能な先頭の桁番号をY（この実施例では32）とする（ステップ807、808）。内部メモリのモードに切換え、カウンタ内容をXに設定して、カウンタ内容に所定する内部メモリの始かゝるカウンタ内容に所定する内部メモリに格納する（ステップ808～812）。この処理は、この実施例では桁番号番組CPU51により制御される。その処理の後は、ステップ813、再びカウンタ内容Xを出力し、対応する内部メモリの始の番組データを読み出す（ステップ814）。この処理は、この実施例では、CPU51により制御される。

タ内容やから、意図を引いて、新たなカウンタリング
 内容に対してはICカードの所に、バックアップメモ
 リに格納した暗号データを記録して、記録の終了
 を待つ（ステップP837-P837）。ス
 テップP832に遷り、次の暗号処理に移る。
 ステップP834の処理で $X=0$ 、すなわち暗
 号メモリに記憶された全ての暗号データの処理が
 終了したときは、ICカードに記憶格納された暗号や
 暗号メモリに格納されていた暗号データを引出
 して、暗号メモリに格納されていた暗号データをこ
 との暗号等やICカードへの記憶処理であるこ
 とを指示して処理を終了する（ステップP840
 -P841）。

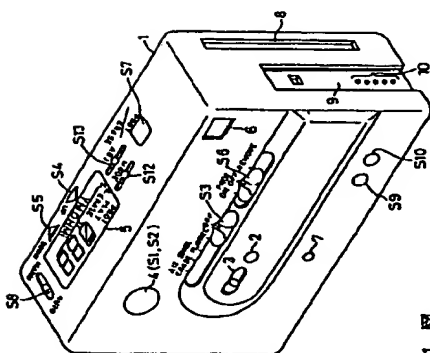
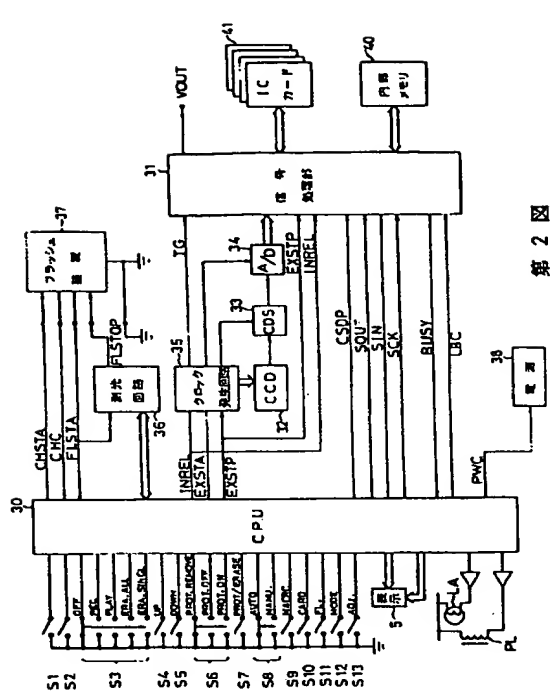
なお、上記要領では、内務省より記録される
てゐる調査を基に、ICカードは未記録のものに属
されるが、一面に調査データの記録されている
ICカードの未記録部分に記録するにしても
ない、また、上記要領では内務省より記録さ
れてゐる全部の調査票をICカードに付してい
るが、プロシチナされてゐる別の調査票の付すよ
うにしてもよい。

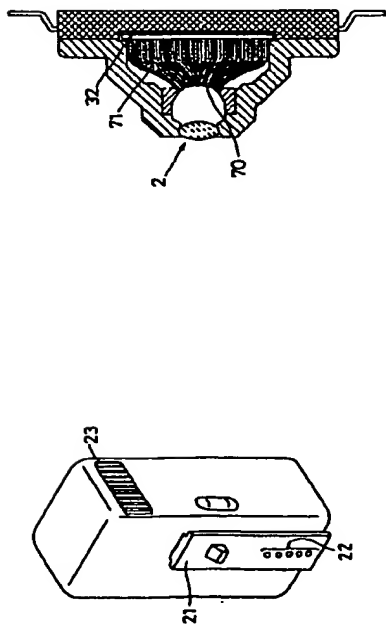
チップP814～P815)、液晶駆動の終了を
検出して(ステップP816)、ICカードモード
を設定し、カウンタ内容をYに設定して、カウン
タ内蔵メモリに対応するICカードの間に、パワ
プ817～P820)、記憶駆動データ記憶する(スチ
ップP821)、再び内部メモリモード
を設定し、駆動すべき内部メモリの装置番号Xから
1を差し引いた次の装置の駆動値をする(ス
チップP822～P823)、装置番号0が否か
を判定し、0でない場合は処理すべき装置があるこ
とを意味するから、カウンタに新しい装置番号Xを
セットし、カウンタ内容Xに対応する内部メモリ
の装置番号データを読み出して(ステップP827)、そ
れを格納する(ステップP824～P827)。その
液晶駆動の終了を検出して(ステップP828)、再び
カウンタ内蔵メモリを出力し、対応する内部メモリの
装置番号データを読み出す(ステップP829～
P830)、液晶駆動の終了を待って(ステップ
P831)、ICカードモードを設定し、カウン

[illegible]

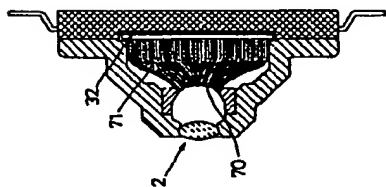
第19段 (a) (b) (c) は記号カードの組合の表示例を示し、(a) はICカードが抽出されてICカードが読まれ、3枚の暗号記号が可読であることを示している。(b) はICカードの金銭が記号所で可読であることを示している。(c) はICカードが読まれ、暗号メモリに10枚の暗号の記号が可読であることを示している。(d) はICカードが読まれ、暗号メモリに10枚の暗号の記号が可読であることを示している。

— 196 — 圖 61 第

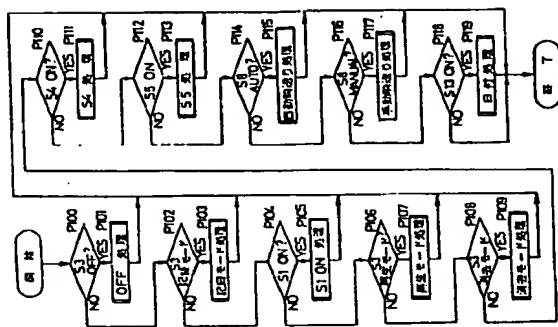




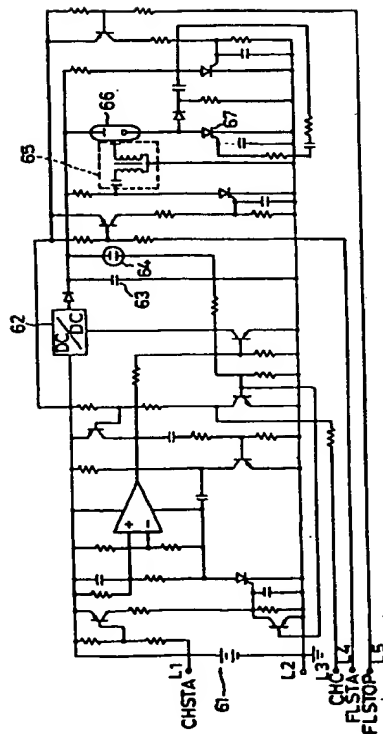
第4図



第6図

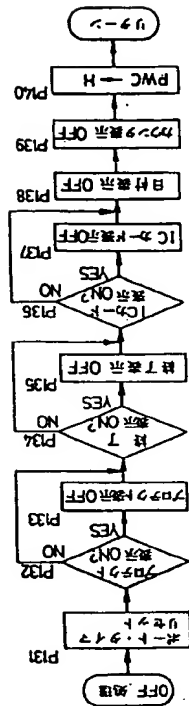


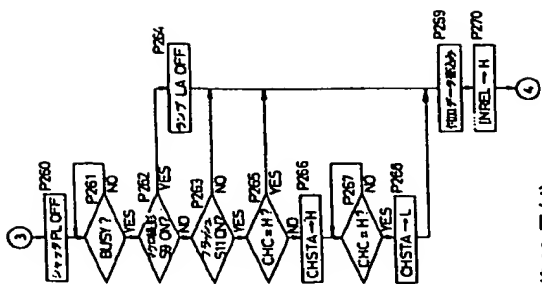
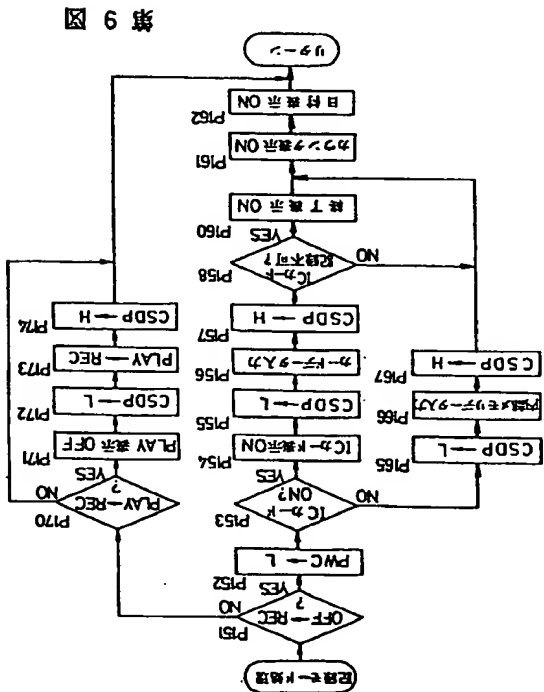
第7図



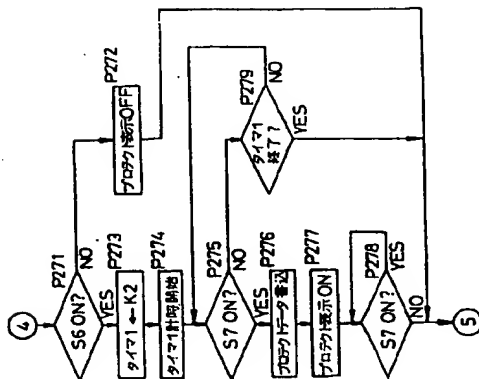
第5図

第8図

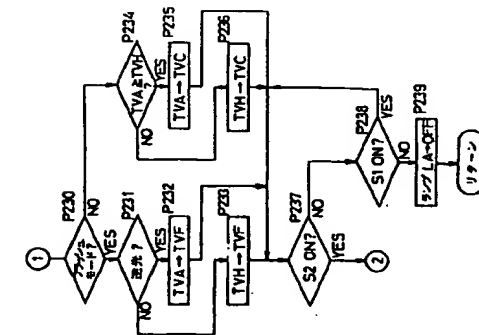


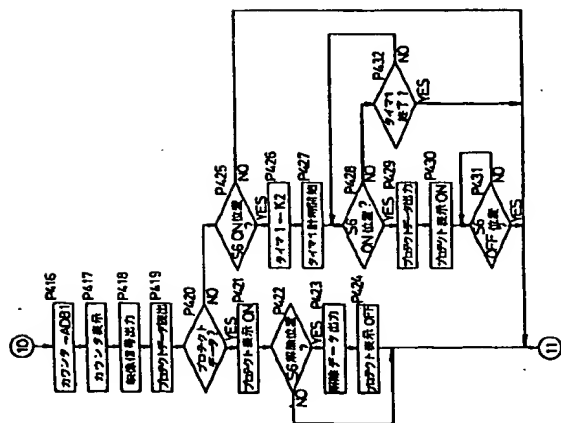


第 10 図 (c)

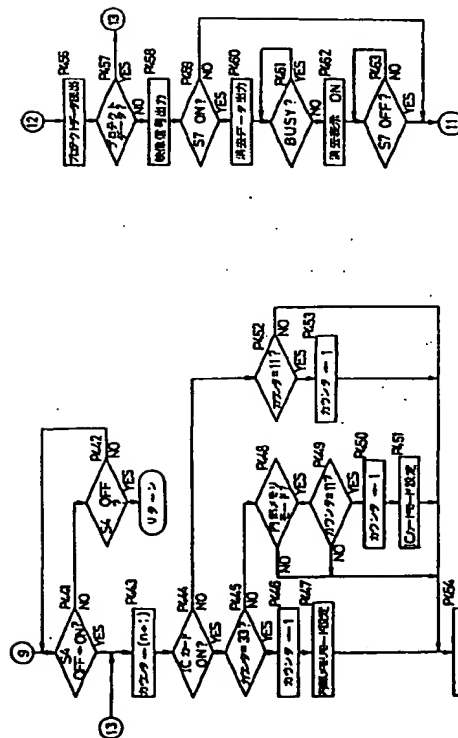


第 10 図 (e)

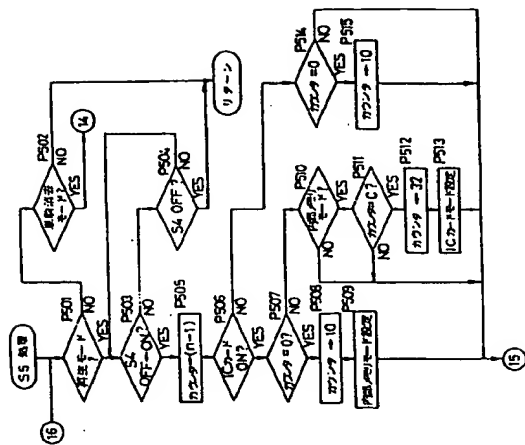




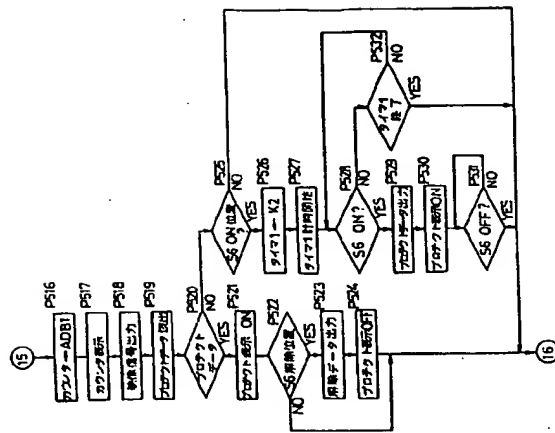
第 13 図 (b)

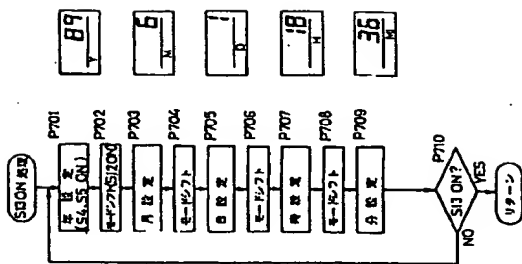


第 13 図 (c)

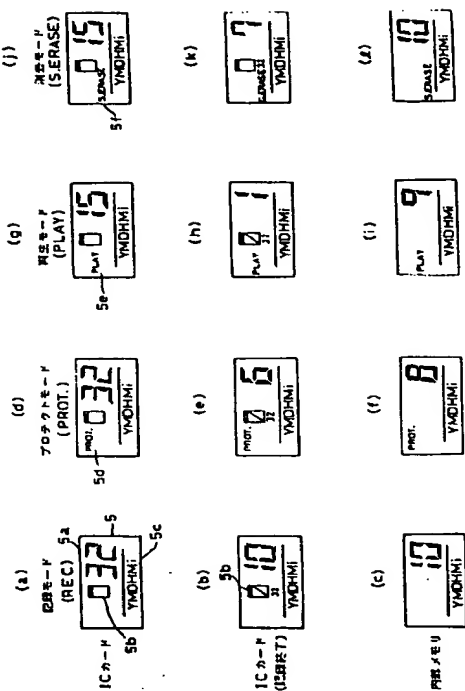


第 14 図 (a)



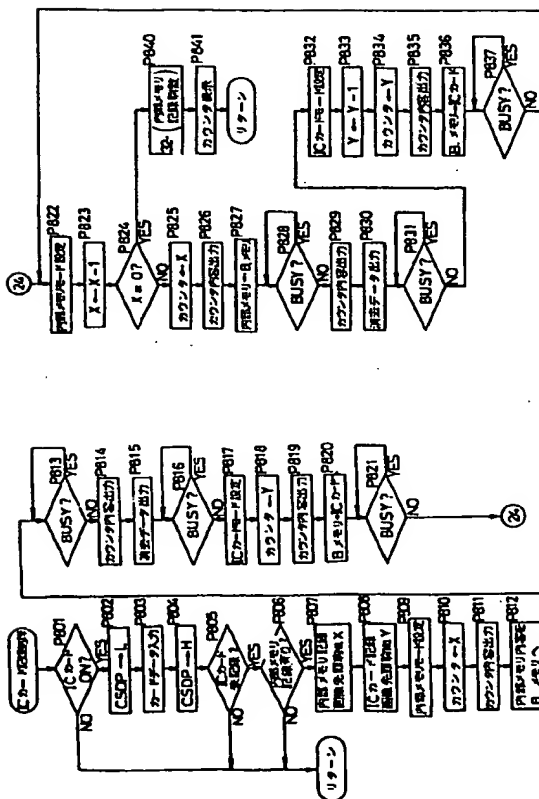


第16圖



19 题

第 18 圖 (a)



第18圖(b)

三、

【この巻頭、上野の雑草が中心である。雑草という表現は、多くの人に

【註 2】

1

[illegible]

13

[illegible]

特開平4-78280

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【部門区分】第7部門第3区分

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【公開日】平成4年(1992)3月12日

(年通号数) 公明特許公報 4-783

【出版番号】特選平2-188117

【國際特許分類第8版】

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5/78

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(13)

DBL/S
NOTES

TS/S

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「理」



Japanese Patent Application Laid-Open No. 4-78280(1992)

SPECIFICATION

5 1. Title of the Invention

Still video camera provided with removable recording medium

2. Claim

A still video camera provided with a recording medium detachably
10 attached thereto, which comprises a first image recording medium that
has an image recording area corresponding a plurality of frames and is
placed inside the camera, and a second image recording medium that has
an image recording area and is freely detachably attached to a camera
main body, characterized by comprising:

15 detection means for detecting an attached state of said second
image recording medium to the camera main body; and

control means which, upon detection of said second image
recording medium being attached to the camera main body by said
detection means, transfers image signals recorded in said first image
20 recording medium to a recordable area of said second image recording
medium to be recorded therein.

3. Detailed Description of the Invention

[Technical Field of the Invention]

25 The present invention relates to a still video camera which

converts a still image into an electric signal and records the signal in an electronic recording medium.

[Prior Art]

In still video cameras, there has been proposed an arrangement in which, after an image has been recorded in a recording medium, for example, an IC card, that is freely detachably attached to the camera, this is taken out and attached to another reproducing device, that is, a CRT display device, a printer, etc., so as to reproduce the recorded image.

Moreover, there has been proposed another arrangement in which, in addition to a recording medium such as an IC card, an inner memory is provided in the camera so that, even when the recording medium such as an IC card is not attached, an image recording process can be carried out.

[Problems to be Solved by the Invention]

In the above-mentioned conventional still video cameras, in the latter cameras, in order to reproduce the image recorded in the inner memory, it is necessary to connect the camera main body to a CRT display device or a printer, and this operation causes inconvenience in its operability.

Therefore, an objective of the present invention is to solve this problem.

[Means for Solving the Problems]

In order to solve the above-mentioned problem, this invention provides an arrangement which can transfer image signals recorded in the inner memory to a detachably attached recording medium such as an IC card to be recorded therein, and in this arrangement, a still video

camera, which is provided with a first image recording medium that has an image recording area corresponding a plurality of frames and is placed inside the camera, and a second image recording medium that has an image recording area and is freely detachably attached to a camera main body, is characterized by comprising: a detection means for detecting an attached state of the second image recording medium to the camera main body; and a control means which, upon detection of the second image recording medium being attached to the camera main body by the detection means, transfers image signals recorded in the first image recording medium to a recordable area of the second image recording medium to be recorded therein.

[Function]

When the second image recording medium, which can be detachably attached to the camera main body, is attached to the camera main body, image signals, stored in the first image recording medium placed inside the camera main body, is read out and recorded in a recordable area in the second image recording medium. Thus, the image recording signals recorded are all stored in the detachably attached recording medium, and can be taken out from the camera main body.

[Preferred Embodiments of the Invention]

Referring to Figures, the following description will discuss preferred embodiments of the present invention. Fig. 1 is a perspective view that shows the external appearance of a camera in accordance with the present invention; and reference number 1 is a camera main body, 2 is a pickup lens, 3 is an open-close knob for a lens protective barrier, 4 is a

shutter button which, when pressed to the first stage, allows a switch S1 which will be described later to close, and when pressed to the second stage, allows a second switch S2 to close.

Reference number 5 is a display section which displays the
5 number of a frame of a recorded image, the presence or absence of an IC card, the date, and other operation states of the camera. Reference number 6 is a finder window, 7 is a light projection window for a macro pickup process, 8 is a slot for an IC card in which images are recorded, 9 is a connecting section of a flash device, and 10 is a connecting-use contact
10 for the camera main body and the flash device. Next, an explanation will be given of an operation switch. S3 is a sliding mode-switching switch for switching various functions provided in the camera, and the selectable modes are described as follows:

OFF: a mode for inhibiting the activation of the camera.

15 REC: a recording mode in which an image is recorded in the inner memory of the camera or the external recording medium that is detachable attached thereto (hereinafter, referred to as IC card).

PLAY: a reproducing mode in which images, recorded in the inner memory or the IC card, are reproduced, and image signals are outputted.

20 Based upon these signals, a recorded image is reproduced on a video display device, not shown.

ERASE-ALL: an erasing mode in which all the images recorded in the inner memory and the IC card are erased.

ERASE-SINGL: a single-frame erasing mode in which a single frame of a
25 picked-up image recorded in the inner memory or the IC card is erased.

Even in this mode, an image protected by a protect function which will be described later is not erased.

S4 and S5 are access switches, and switch S4 (UP) functions as a forwarding switch of recorded images at the time of an image reproducing
5 process, and also functions as a switch for incrementing the date at the time of a date-setting process. Moreover, switch S5 (DOWN) functions as a rewinding switch of recorded images at the time of the image reproducing process, and also functions as a switch for decrementing the date at the time of the date-setting process.

10 S6 is a protect switch used for protecting a necessary image from being erroneously erased among images recorded in the inner image or the IC card, and is indicated as "PROT". In the case when switch S6 is in OFF position, the protective function is not operative, and when it is in ON position, the protective function becomes operative. Moreover, when
15 it is in REMOVE position, that is, in a releasing position, a protected state of an image that has been protected is released.

S7 is a protect/erase operation switch, and when this switch is turned on with the mode switching switch S3 being in ERASE position (either SINGL or ALL position), the erasing operation is carried out, and
20 when this switch is turned on with the protect switch S6 being in PROT position, the protective operation is executed.

S8 is a frame-forwarding switch for making switches between an automatic frame-forwarding process and a manual frame-forwarding process at the time of reproducing the recorded images, and each time
25 this is switched to AUTO, that is, the automatic process, the recorded

images are automatically frame-forwarded and successively reproduced every constant time without the need of operating the access switch S4 or S5. Moreover, when this is switched to MANUAL, that is, the manual process, the recorded images are frame-forwarded frame by frame by the operation of the access switch S4 or S5.

S9 is a macro-pickup switch, and S10 is a switch for setting a flash pick-up process.

S12 is a date-setting mode switch, each time this is turned ON, modes are switched cyclically in the order of Y (year)—M (month)—D (date)—H (hour)—M1 (minute)—Y (year).

S13 is a date setting switch which sets data selected by the switch S12.

Fig. 2 is a block diagram that shows a camera control circuit.

Reference number 30 is a CPU for controlling the entire camera, and 31 is a signal processing section for carrying out recording and reproducing operations on image signals. These processes will be described later in detail. Reference number 32 is a solid-state pickup element (hereinafter, referred to as CCD) constituted by CCDs, etc., and this converts an image that has been made incident thereon through the pickup lens 2 into an image signal. Reference number 33 is a correlation double sampling section for the image signal outputted from the CCD, 34 is an A/D converter for converting the image signal to a digital signal, 35 is a clock generation circuit for synchronizing the CCD 32, the sampling section 33 and the A/D converter 34, and this is controlled by control signals INREL and EXSTP outputted from the CPU 30. Reference

number 36 is a photometer circuit which measures the luminance of a subject, and outputs the results of the measurements to the CPU 30, and which also functions as a light-adjusting circuit for adjusting the light of the flash light. Reference number 37 is a flash device, and is provided
5 with a light-emitting section and a charging capacitor. Reference number 38 is a power supply which is controlled by a control signal PWC outputted from the CPU 30. Reference number 5 is a display section which displays the number of image frames, etc. as described earlier. LA represents an illuminating lamp used at the time of the macro-picking-up
10 process, and PL is an operational electromagnetic plunger.

Reference number 40 is an inner memory that is built in the camera, and has an image recording capacity of at least one frame (10 frames in this preferred embodiment). Reference number 41 is an IC card that is detachably attached to the camera main body, and is provided
15 with a semiconductor memory, such as an SRAM, etc., which has an image storing capacity corresponding to a plurality of frames (32 frames in this preferred embodiment).

Next, an explanation will be given of switches. S1 is a switch which is turned on when the release button 4 is pressed to the second
20 stage, and S2 is a switch which is turned on when the release button 4 is pressed to the second stage. S3 to S9 as well as S11 to S13 are switches whose operation sections are placed on the camera main body shown in Fig. 1, and referring to Fig. 1, their functions have been described earlier. S10 is a switch which is turned on when the IC card 41 is inserted
25 through the inserting section 8 of the camera main body, and outputs a

signal indicating the insertion of the IC card 41.

Next, an explanation will be given of signals that are transmitted through signal lines.

CHSTA is a signal for giving an instruction so as to charge the capacitor of the flash device 37, CHC is a signal for indicating the completion of the charging of the capacitor of the flash device 37, FLSTA is a signal for giving an instruction so as to make the flash device 37 emit flash light, and FSTOP is a signal for giving an instruction so as to stop the flash light emission when the quantity of flash light detected by the photometer circuit 36 has reached a predetermined value (upon completion of the light adjustment).

INREL, which is a shutter release starting signal, is outputted from the CPU 30 to the clock generation circuit 35. In response to this signal, the clock generation circuit 35 outputs a signal EXSTA for indicating the start of exposure control to the CPU 30. EXSTP, which is an exposure control completion signal, is outputted from the CPU 30 to the clock generation circuit 35. Moreover, the shutter release starting signal INREL and the exposure control completion signal EXSTP are also outputted to the signal processing section 31, which will be described later.

CSDP is a signal for controlling the signal transfer process between the CPU 30 and the signal processing section 31, SOUT and SIN are data signals that are transferred as serial data between the CPU 30 and the signal processing section 31, SCK is a serial clock signal transferred from the CPU 30 to the signal processing section 31, BUSY is

a signal for informing the CPU 30 that the signal processing section 31 is processing signals, LBC is a signal for indicating that a macro-pickup process is to be executed, and VOUT is an image signal outputted from the signal processing section 31.

5 Fig. 3 is a block diagram that indicates the signal processing section 31 in detail. Reference number 51 is a signal processing CPU for executing the entire control of the signal processing section 31, 52 is a signal processing circuit for processing the image signal (including a compressing process), and 53 is an address generation circuit for
10 generating an address signal upon receipt of the clock signal from the clock generation circuit 35.

 Reference number 54 is a multiplexer which, based upon the signal RD/CD outputted from the signal processing circuit 52, selects either of the address signals outputted from the address generation
15 circuit 53, that is, either of an address signal bus used for recording the image signal outputted from the CCD 32 in the buffer memory 55 and an address signal bus used at the time when the buffer memory 55 is used for the signal processing operation.

 Reference number 56 is a multiplexer which, based upon the
20 signal D1/D2 outputted from the signal processing CPU 51, selects either of an address signal bus ADB1 outputted from the signal processing circuit 52, that is, an address signal bus used when the image signal is recorded and reproduced on and from the image recording inner memory 40 and the IC card 41, and an address signal bus ADB2 used in the case
25 when a data signal other than the image signal outputted from the signal

processing CPU 51, that is, for example, a frame number, protect data, etc., is recorded in the inner memory 40 and the IC card 41.

Reference number 57 is a multiplexer which, based upon the signal D1/D2 outputted from the signal processing CPU 51, selects either
5 of an image signal bus DB1 and a data signal bus DB2 other than the image signal such as a frame number, protect data, erasing data (ERASE), protect removing data (REMOVE) and chronodata.

Moreover, reference number 58 is a D/A converter which converts a digital signal to an analog signal at the time of outputting the image
10 signal.

Next, an explanation will be given of signals transferred by signal lines. Among signals outputted from the signal processing CPU 51, ENA is a signal for allowing the signal processing circuit 52 to carry out the signal processing, REC/PLAY is a signal for controlling the signal
15 processing circuit 52 as to whether the signal processing is carried out in the recording mode or in the reproducing mode, RE/WR is a signal for controlling the write/read processing of the image signal to be carried out on the inner memory 40 and the IC card 41, ERASE is a signal for controlling the erasing operation on the image signals recorded in the
20 inner memory 40 and the IC card 41, CSOUT is a signal for controlling data communication to be carried out on the IC card 41, and CSIN is a signal for controlling data communication to be carried out on the inner memory 40.

Fig. 4 is a perspective view that shows the external appearance of
25 the flash device that is detachably attached to the camera in accordance

with the present invention. A connecting electric contact 22, which is placed in a connecting section 21 that is engaged by the connecting section 9 of the flash device of the camera main body 1, is allowed to contact the electric contact 10 of the camera main body 1. Reference number 23 represents a light-emitting section.

Fig. 5 shows a circuit diagram of the flash device. This circuit is a known circuit, and an explanation will be briefly given of the constitution and operation of this circuit. In this Figure, reference number 61 is a power supply battery, 62 is a voltage-raising circuit constituted by a DC/DC converter, 63 is a main capacitor used for accumulating charge, 64 is a neon tube, 65 is a trigger circuit, 66 is a xenon discharging tube, and 67 is a thyrister.

Next, an explanation will be given of the operation thereof. When the signal CHSTA for giving an instruction for the start of discharging, which is applied to the terminal L1 from the CPU 30 of the camera, is allowed to go "High", the voltage-raising circuit 62 starts its operation so that the voltage of the battery device 61 is increased so as to charge the main capacitor 63. When the terminal voltage of the main capacitor 63 has reached a predetermined value, the signal CHC to be outputted to the terminal L3 is allowed to go "High", thereby informing the CPU 30 of the completion of charging. When the signal FLSTA for giving an instruction for the light emission of the flash, which is applied to the terminal L4 from the CPU 30 of the camera, is allowed to go "High", the trigger circuit 65 is operated so that the xenon discharging tube 66 starts emitting light. The photometer circuit 36 of the camera detects

reflected light from a subject, and when the quantity of light has reached a predetermined value, a light-emission stopping signal FLSTP, which is applied to the terminal L5, is allowed to go "High" to apply a reverse bias voltage to the thyristor 67, thereby stopping the light emission.

5 An explanation will be given of the constitution of the image pickup section. Fig. 6 is a cross-sectional view taken along a plane including the light axis of the image pickup section; and reference number 2 is a spherical lens having a focal length f , 70 is an image-converging face of the lens 2 having a spherical shape. Reference
10 number 71 is an optical fiber, and its light incident end is placed along the spherical image-converging face 70 while its light-releasing end is arranged on the surface of the CCD 32. When the optical fiber 71 has an enlarging rate of 3 times, it is possible to converge the same image as a converged image on the CCD 32 derived from an image having a size of
15 the focal length $f \times 3$. In this manner, the application of an optical fiber having an enlarging rate of several times, the thickness of the image pickup section can be made thinner to the dimension (for example, 3 mm) of the lens focal length and the optical fiber section, and the combination of this with the IC card makes it possible to provide a thinner camera
20 main body.

 Here, the advantages of the application of a spherical lens as the image pickup lens are described as follows: In general, when an image of an object located at point of infinite is converged by using a spherical lens, the image-converging face has a spherical face that is concentric
25 with the spherical lens because of the spherical symmetric property of the

spherical lens. Therefore, in the spherical lens, aberrations on the axis and out of the axis have an identical value so that when a virtually optimal aberration correction is achieved on the axis, the aberration out of the axis is also corrected. Therefore, although it is a simple, smaller
5 optical system as compared with the common lens system, by applying a proper aberration correction thereto, it becomes possible to obtain a lighter lens that has a superior light-converging property, and is less susceptible to a reduction in the peripheral quantity of light.

Referring to flow charts shown in Figs. 7 to 17, an explanation will
10 be given of the controlling operation of the camera executed in the CPU 30.

Fig. 7 is a flow chart showing the outline of the entire controlling operation, and this shows that a check is made to see the state of each of the switches and the sequence proceeds to the corresponding processing
15 routine. Upon start of the controlling operation, a check is first made to see whether or not the mode switching switch S3 is set to OFF position, and in the case when it is located at OFF position, the sequence proceeds to a routine for the OFF processing (step P100, P101). A check is made to see whether or not the mode switching switch S3 is set to REC, that is,
20 the recording mode, and if it is in the recording mode, the sequence proceeds to the routine for the recording-mode processing (step P102, P103). A check is made to see the state of the switch S1 that is turned ON when the shutter release button is pressed to the first stage, and if this is ON, the sequence proceeds to a S1 ON processing routine (step
25 P104, P105). A check is made to see whether or not the mode switching

switch S3 is set to PLAY, that is, the reproducing mode, and when set to the reproducing mode, the sequence proceeds to a reproducing-mode processing routine (step P106, P107). A check is made to see whether or not the mode switching switch S3 is set to ERASE, that is, the erasing
5 mode, and when set to the erasing mode, the sequence proceeds to an erasing-mode processing routine (step P108, P109). A check is made to see the state of the access switch S4 (UP), and when set to ON, the sequence proceeds to a S4 processing routine (step P110, P111). A check is made to see the access switch S5 (DOWN), and when set to ON, the
10 sequence proceeds to S5 processing routine (step P112, P113). A check is made to see whether or not the frame-forwarding switch S8 is set to AUTO, that is, the automatic mode, and when set to the automatic mode, the sequence proceeds to an automatic mode processing routine (step P114, P115). A check is made to see whether or not the frame-forwarding
15 switch S8 is set to MANUAL, that is, the manual mode, and when set to the manual mode, the sequence proceeds to a manual mode processing routine (step P116, P117). A check is made to see the state of the date setting switch S13, and when this is set to ON, the sequence proceeds to a date-processing routine (step P118, P119).

20 Fig. 8 shows a processing routine that corresponds to the routine with the mode switching switch S3 being OFF that is shown as the step P101 of the flow chart of Fig. 7. First, respective ports and timers are reset (step P131), and a judgment is made as to whether or not the display section indicating that the protective function is in operation is
25 set to ON, and when set to ON, the display is turned OFF (step P132,

P133). A judgment is made as to whether or not the completion display indicating that the number of frames of the recorded images has reached a recordable number of frames is ON, and when this is ON, the display is turned OFF (step P134, P135). A judgment is made as to whether or not
5 the display, which indicates that the IC card 41 is inserted in the camera main body, is turned ON, and when this is ON, the display is turned OFF (step P137), the date display is turned OFF, the counter display indicating the number of frames of recorded images is turned OFF (step P138, P139), the power supply circuit is cut off with the signal PWC being
10 "High" to the power supply 38 (step P140), the sequence proceeds to the main routine.

Fig. 9 shows a processing routine that corresponds to the recording-mode processing routine with the mode switching switch S3 being in the recording mode (REC) that is shown as the step P103 of the
15 flow chart of Fig. 7. First, a judgment is made as to whether or not the mode switching switch S3 has been switched from OFF to REC position (step P151), and when switched thereto, the signal PWC is allowed to go "Low" to turn the power supply 38 ON (step P152). A judgment is made as to whether or not any IC card 41 is inserted in the camera (step P153),
20 and when it is inserted, the IC card display is turned ON (step P154), and the signal CSDP is allowed to go "Low" so that card data indicating the recording state (the number of recorded frames, etc.) of the IC card 41 is received from the signal processing CPU 51, and after the completion of the communication, the signal CSDP is allowed to go "High", thereby
25 completing the communication (step P155, P156 and P157). A judgment

is made as to whether or not the recording section of the IC card 41 is full so that recording is no longer made (step P158), and when no recording is available, the display of completion is turned ON, the counter display indicating the number of recordable frames is turned ON and the data
5 display is turned ON (step P160, P161, P162); thus, the sequence returns to the main routine. At the time of the judgment in step P158, if there is any unrecorded section on which recording is made, the step P160 is omitted.

If the judgment at step P153 shows that no IC card 41 is inserted,
10 the signal CSDP is allowed to go "Low" so that memory data, which indicates the recorded state (the number of recorded frames, etc.) of the inner memory 40, is received from the signal processing CPU 51, and after the completion of the communication, the signal CSDP is allowed to go "High", thereby completing the communication (step P165, P166 and
15 P167), and the sequence proceeds to step P161.

If the judgment at step P151 does not show the switching from OFF to REC, a judgment is made as to whether or not the mode switching switch S3 is switched from PLAY to REC (step P170), and if switched thereto, the display of PLAY on the display section is turned OFF, and the
20 signal CSDP is allowed to go "Low" so that a signal indicating that the switching has been made from PLAY to REC is outputted to the signal processing section, thereby making the signal CSDP go "High" to complete the communication signal (step P171, P172, P173 and P174); thus, the sequence returns to the main routine.

25 Figs. 10(a) to 10(f) show a processing routine that corresponds to

the processing routine shown as step P105 of Fig. 7, in which the switch S1, which is turned on upon pressing of the release button to the first stage, is turned ON. First, a judgment is made as to whether or not the recording mode (REC) is maintained (step P201). If it is not the recording mode, the display of the display section 5 is flickered so as to indicate that no image pickup is available, and after switch S1 has been turned OFF, the sequence returns to the main routine (step P207, P208).

If the judgment at step P201 shows the recording mode, a judgment is made as to whether or not the frame-number display counter of the recorded images is zero (step P202), and if this is zero, a predetermined value K1 is set in the timer 1 to start it to count time in order to show that image recording is no longer available, and the counter display is flickered (step P203, P204). Upon completion of the time counting of the timer 1, the counter display is switched to a continuous light-on display (step P205, P206); thus, the sequence proceeds to the main routine.

If the judgment at step P202 shows that the counter is not zero, that is, the image pickup is available, the sequence proceeds to step P210 and thereafter. First, a judgment is made as to whether or not the macro pickup switch S9 is turned ON, and if this is ON, the macro pickup lamp LA is turned on (step P210, P211). If it is not the macro pickup process, the step P211 is omitted. The luminance of the subject, measured by the photometer circuit 36, is A/D converted and inputted (step P212), and a judgment is made as to whether or not the macro pickup switch S9 is turned on (step P213), and if this is ON, the sequence proceeds to P230.

If the macro pickup switch S9 is not ON, a judgment is made as to whether or not the subject is subjected to any of counter light or low luminance (step P214, P215), and if neither counter light nor low luminance occurs, the sequence proceeds to step P230. In the case of
5 counter light or low luminance, a judgment is made as to whether or not the flash pickup switch S11 is turned ON (step P216), and if this is ON, a judgment is made as to whether or not the signal CHC indicating the completion of charging of the main capacitor 63 of the flash device 37 is “High” (step P217), and if this is “High”, the sequence proceeds to step
10 P230. Moreover, if it is not “High”, the signal CHSTA for giving an instruction so as to start charging the main capacitor is allowed to go “High” to start charging, and after the charging process has been completed, the signal CHSTA is allowed to go “Low” to stop the charging (step P219, P220, P221), and a check is made to see whether the switch S1
15 is ON or not, if this is ON, the sequence proceeds to step P230, and if this is not ON, the sequence returns to the main routine.

A judgment is made as to whether or not the flash mode is ON at step P230. If the flash mode is ON, a judgment is made as to whether or not counter light occurs, and if counter light occurs, the shutter speed
20 TVA, determined by the luminance of the subject, is switched to the flash controlling shutter speed TVF, and if no counter light occurs, the shutter speed TVH, determined by the hand trembling limit, is switched to the flash controlling shutter speed TVF (step P231, P232, P233). The judgment at step P230 shows that it is not the flash mode, the shutter
25 speed TVA determined by the luminance of the subject and the shutter

speed TVH determined by the hand trembling limit are compared with each other in their values, and in the case of $TVA \geq TVH$, TVA is used as the exposure controlling shutter speed TVC, and in the case of $TVA < TVH$, the TVH is used as the exposure controlling shutter speed TVC (step P234, P235, P236).

A judgment is made as to whether or not the switch S2, which is turned on upon pressing of the release switch to the second stage, is ON (step P237), and if this is not ON, a check is made to see the switch S1, and if this is ON, the sequence returns to step P237, and if this is not ON, the macro pickup lamp LA is turned OFF (step P238, P239), thereby returning to the main routine.

If the judgment at step P236 shows that the switch S2 is ON, a shutter operating plunger PL is turned ON so as to start the exposing operation, and the release start signal INREL is first allowed to go "Low" so as to inform the clock generation circuit 35 and the signal processing section 31 of the start of release (step P240, P241, P242). A judgment is made as to whether or not the macro pickup switch S9 is ON, and if this is ON, the signal LBC is allowed to go "Low" so that the correction in the signal processing in the signal processing section 31 is switched to a WB, γ correction used for the pickup process using a lamp, and if this is not ON, the signal LBC is allowed to go "High" so that it is switched to a WB, γ correction used for the normal pickup process (step P234, P244, P245).

After the exposure start signal EXSTA outputted from the clock generation circuit 35 has been allowed to go "Low" (step P246), a

judgment is made as to whether or not the flash mode is ON (step P 247).

If this is not the flash mode, that is, if the normal pickup process is carried out, based upon the shutter speed TVC at the time of the normal pickup process previously found, a value 2^{TVC} is set to the timer 2, thereby starting to count time. Upon completion of the time counting
5 (step P248, P249, P250), the sequence proceeds to step P260.

In the case when the judgment at step P247 shows that the flash mode is ON, based upon the shutter speed TVF at the time of the flash pickup process previously found, a value 2^{TVF} is set to the timer 2, thereby starting to count time (step P251, P252). A value for specifying
10 the light emission timing of the flash device is set to the timer 3, thereby starting time counting (step P253, P254). Upon completion of the time counting of the timer 2 prior to the timer 3 (for example, in the case when strong light enters during the exposure), the exposure is completed without the light emission of the flash, and the sequence proceeds to step
15 P260. Moreover, upon completion of the time counting of the timer 3 prior to the timer 2, the flash device is allowed to emit light, and the light is adjusted and controlled, and the light emission is stopped, thereby completing the exposure (step P255, P256, P257, P258); thus, the sequence proceeds to step P260.

20 The shutter operating plunger PL is turned OFF (step P260), and the sequence waits for the completion of the signal processing in the signal processing section 31 (step P261). A judgment is made as to whether or not the macro pickup switch S9 is ON (step P262), and if this is ON, the lamp LA is turned OFF (step P264), and the sequence proceeds
25 to step 269, and if it is OFF, a judgment is made as to whether or not the

flash pickup switch S11 is ON. If the switch S11 is OFF, the sequence proceeds to P269, and if this is ON, a judgment is made as to whether or not the signal CHC, which indicates the completion of charging in the main capacitor 63 of the flash device 37, is "High" (step P256), and if this is "High", the sequence proceeds to step P269. If the signal CHC is not "High", the signal CHSTA for giving an instruction so as to start charging the main capacitor is allowed to go "High", thereby starting to charge, and after the completion of the charging, the signal CHSTA is allowed to go "Low", thereby stopping the charge (step P266, P267, P268).

Additional data, such as date data, etc., is recorded in the inner memory 40 and the IC card 41 through the data bus DB2, and the signal INREL for indicating the completion of exposure is allowed to go "High" (step P269, P270).

A judgment is made as to whether or not the protect switch S6 is set to ON position (step P271), and if this is not ON, the protect display is turned OFF (step P272), and the sequence proceeds to step P280. If this is ON, a predetermined value K1 is set to the timer 1, thereby starting to count time (steps P273 to P275). A judgment is made as to whether or not the protect/erase operation switch S7 is turned ON during the counting time of the timer 1 (step P275), and if this is ON, protect data is recorded in the inner memory 40 or the IC card 41 through the data bus DB1 in order to protect the image frame picked up immediately before so that the protect display is turned ON, and after the protect/erase operation switch S7 has been turned OFF (step P276, P277, P278), the sequence proceeds to step 280. Moreover, in the case when the judgment

at step P275 shows that the switch S7 is not ON, that is, in the case when the protect/erase operation switch S7 has not been pressed during the time counting of the timer 1, after the time counting of the timer 1 has been completed, the sequence proceeds to step P280 after completion of
5 the time counting of the timer 1 (step P279), without carrying out the protective process.

After the content of the frame counter has been decremented by one, a judgment is made as to whether or not the content of the counter is zero, and a judgment is further made as to whether or not any IC card
10 has been inserted (step P280, P281, P282). If the counter is not zero, and if any IC card has not been inserted, the sequence proceeds to step P286. If the counter is zero with the IC card being inserted, the content of the counter is set to 10 (the image recording capacity of the inner memory 40) since the IC card is no longer allowed to record, and the
15 completion display of the IC card recording is turned ON (step P283, P284, P285). The image data corresponding to the frame number of the counter is read from the inner memory through the address bus ADB1, and data indicating that the frame is protected or not is inputted (step P286, P287). A judgment is made as to whether or not the frame has the
20 protect data already written thereon (step P288), and if it has the protect data, the sequence returns to step P280 since the frame is not recorded, and the next frame is subjected to the process.

As a result of the judgment at step P288, in the case when the protect data has not been written therein, after the switch S1, which is
25 turned ON upon pressing of the release button to the first stage, has been

turned OFF (step P289), a judgment is made as to whether or not the protect switch S6 is ON (step P290), if it has been turned off. In the case when the switch S6 is ON, a predetermined value K1 is set to the timer 1, thereby starting to count time, and after the protect display has been
5 flickered for a predetermined time, it is continuously lit on, thereby informing that the protect process has been completed (step P291 to P294); thus, the sequence proceeds to step P296. In the case when the judgment at step P290 shows that the protect switch S6 is OFF, the protect display is turned OFF, and after displaying the number of
10 recordable frames on the counter (step P295, P296), the sequence returns to the main routine.

Fig. 11 shows a flow chart of a reproducing-mode processing routine in the case when the function switching switch S3 is in the reproducing mode (PLAY) that is shown as step P107 in the flow chart of
15 Fig. 7. First, a judgment is made as to whether or not the function switching switch S3 has been switched from REC to PLAY position (step P301), and if it has been switched to that position, the PLAY display is turned ON, and the signal CSDP is allowed to go "Low" to inform the signal processing section 31 that the switching to the PLAY mode has
20 been made, and the signal CSDP is allowed to go "High", thereby completing the communication (step P302 to P305). In the case when the judgment at step P301 does not show that the switch S3 has been switched to REC to PLAY, a judgment is made as to whether or not the mode switching switch S3 has been switched from ERASE to PLAY (step
25 P306), and if the switching has been made, the ERASE display is turned

OFF; thus, the sequence proceeds to step P302. Moreover, if the switching has not been made, the sequence proceeds to step P308.

A judgment is made as to whether or not any IC card 41 has been inserted (step P308), and if any IC card 41 has been inserted, the card
5 display is turned ON, and a judgment is made as to whether or not the IC card has just been inserted during the reproducing mode. If it has just been inserted, the number of reproducible frames 32 is set on the counter, and the card mode is set (steps P309 to P312). If the judgment at step P310 shows that the IC card has already been inserted, the processes
10 such as setting of the number of reproducible frames (steps P311 and P312) are omitted. If the judgment at step P308 shows that no IC card is inserted, the card display is turned OFF, and a judgment is made as to whether or not the IC card has just been drawn therefrom, and if it has just been drawn, the number of reproducible frames 10 is set on the
15 counter, and the inner memory mode is set (steps P313 to P316). If the judgment at step P314 shows that the IC card was previously drawn, the processes such as the setting of the number of reproducible frames (steps P315 and P316) are omitted.

The contents of the counter are outputted through the address bus
20 ADB1 so that the contents of the counter are displayed, and image data at the corresponding address is read from the IC card 41 or the inner memory 40, and outputted as image signals (step P317 to P319). When the access switch S4 (UP) is pressed, the sequence proceeds to an S4 processing routine, which will be described later, and when the access
25 switch S5 (DOWN) is pressed, the sequence proceeds to an S5 processing

routine, which will be described later. Here, if any selection switch for another mode is pressed, the sequence returns to the main routine, and then proceeds to the corresponding sub-routine (steps P320 to P322). In the case when neither the access switch S4 nor S5 nor any selection
5 switch for another mode is pressed, the sequence returns to step P319, thereby continuing to output the image signals.

Figs. 12(a) to 12(c) show an erasing-mode processing routine in the case when the mode switching switch S3 is in the erasing mode (ERASE) that is shown as step P109 in the flow chart of Fig. 7. First, a
10 judgment is made as to whether or not the mode switching switch S3 is set to ERASE-SINGLE (step P331), and if it is set to ERASE-SINGLE, that is, in the case of the single-frame erasing process, the sequence proceeds to step P332, and if it is set to ERASE-ALL, that is, in the case of the all-frame erasing process, the sequence proceeds to step P371.

15 At step P332, a judgment is made as to whether the mode switching switch S3 is switched from PLAY to SINGLE or from All to SINGLE, and in the former case, the PLAY display is turned OFF, and in the latter case, "A" display indicating all the frames is turned off (steps P332 to P335). "S" display indicating the single frame is turned ON, and
20 the signal CSDP is allowed to go "Low" so as to inform the signal processing CPU 51 that the single frame erasing mode is ON, and the signal CSDP is allowed to go "High", thereby completing the communication (steps P336 to P339).

Next, depending on whether or not any IC card 41 has been
25 inserted, the IC card mode or the inner memory mode is set (step P340 to

P348). The sequence is the same as that of the PLAY processing routine at steps P308 to P316 shown in Fig. 11; therefore, the detailed description thereof is omitted.

The sequence proceeds to step P350, and the contents of the
5 counter is outputted through the address bus ADB1 so that the contents
of the counter are displayed, and the protect data of the image to be
reproduced is read (step P350 to P352). A judgment is made as to
whether or not the image to be reproduced has protect data, and if there
is no protect data, that is, if the data is not protected, the image data is
10 outputted, and if there is protect data, the contents of the counter are
decremented by one, and the processing is executed on the next frame;
therefore, the sequence returns to step P350 (steps P353, P354 and P355).
The above-mentioned processes make it possible to prevent the image
bearing the protect data from being reproduced, and thereby from being
15 erroneously erased.

A judgment is made as to whether or not the protect/erase
operation switch S7 is turned ON (step P356), and if it is ON, the erasing
data is outputted to the signal processing CPU 51 so that after the
erasing process on the recorded image has been completed, the erase
20 display is turned ON (steps P357 to P359). After the protect/erase
operation switch S7 has been turned OFF (step P360), the sequence
proceeds to P361. In the case when the judgment at step P356 shows the
switch S7 is not ON, the sequence also proceeds to step P361.

When the access switch S4 (UP) is pressed, the sequence proceeds
25 to the S4 processing routine, which will be described later, and when the

access switch S5 (DOWN) is pressed, the sequence proceeds to the S5 processing routine, which will be described later. Further, when any selection switch for another mode is pressed, the sequence returns to the main routine, and then proceeds to the corresponding sub-routine (steps
5 P361 to P363). Neither the access switch S4 nor S5, nor any selection switch for another mode is pressed, the sequence returns to step P350.

If the judgment at step P331 shows that not the single-frame erasing but the all-frame erasing is ON, the sequence proceeds to P371. First, “S” display indicating the single frame is turned OFF, and “A”
10 display indicating all the frames is turned ON. The signal CSDP is allowed to go “Low” so as to inform the signal processing CPU 51 that the all-frame erasing mode is ON, and the signal CSDP is allowed to go “High”, thereby completing the communication (steps P371 to P375). A judgment is made as to whether or not the protect/erase operation switch
15 S7 is ON (step P376), and if it is ON, the erasing data is outputted to the signal processing CPU 51, and after the erasing process has been completed, the erase display is flickered. Then, after the switch S7 has been turned OFF, the erase display is turned ON (steps P377 to P381). A judgment is made as to whether or not any IC card 41 has been inserted,
20 and if it has been inserted, the contents of the counter are set to 32, while if it has not been inserted, the contents of the counter is set to 10 (steps P382 to P385), and the sequence returns to the main routine.

Figs. 13(a) to 13(d) are flow charts that show processes, such as a forwarding process of image frames at the time of reproducing the
25 recorded images and a forwarding process of image frames at the time of

erasing images frame by frame, carried out by the operations of the access switch S4 (UP) that is shown as step P111 of the flow chart shown in Fig.

7. First, a judgment is made as to whether or not the mode switching switch S3 is set to the reproducing mode (PLAY) (step P401), and if it is
5 not the reproducing mode, a judgment is made as to whether or not the erasing mode frame by frame (S-ERASE) is ON, and if it is the erasing mode, the sequence proceeds to step P441, and if it is not the erasing mode, the sequence returns to the main routine (step P402).

When the judgment at step P401 shows the reproducing mode, a
10 judgment is made as to whether or not the access switch S4 is switched from OFF to ON, and each time the switching is made from OFF to ON, the sequence proceeds to step P405 (step P403, P404). The contents of the counter are incremented by 1 (step P405), and a judgment is made as to whether or not any IC card 41 has been inserted (step P406). If it has
15 been inserted, a judgment is made as to whether or not the contents of the counter have become 33 (step P407). If the contents of the counter is 33, this indicates that all the frames recorded in the IC card 41 have been reproduced; therefore, the counter is set to 1 so that the inner memory mode is set so as to reproduce the images recorded in the inner memory
20 40 (step P408, P409). If the judgment at step P407 shows that the contents of the counter are not 33, a judgment is made as to whether or not the inner memory mode is set, and if the inner memory mode is set, a judgment is made as to whether or not the contents of the counter are 11 (step P410, P411). In the case when the contents of the counter are 11,
25 this indicates that all the frames recorded in the inner memory 40 have

been reproduced; therefore, the counter is set to 1, and the IC card mode is set so as to reproduce images recorded in the IC card 41 (step P412, P413). If the judgment at step P410 or P411 is negative, the sequence proceeds to step P416. Moreover, if the judgment at step P406 shows
5 that no IC card is inserted, a judgment is made as to whether or not the contents of the counter are 11, and if the contents of the counter are 11, the counter is set to 1, and if not 11, the sequence immediately proceeds to step P416 (step P414, P415).

The contents of the counter are outputted through the address bus
10 ADB1, an access is made to the IC card 41 or the inner memory 40, the contents of the counter are displayed, and the image data in the frame corresponding to the address is read from the IC card 41 or the inner memory 40 so that the resulting data is outputted as image signals (steps P416 to P418). The protect data of the frame being reproduced are read
15 out, and a judgment is made as to whether or not the image being reproduced is protected (step P419, P420). As a result of the judgment, if the data is protected, the protect display is turned ON, and a judgment is made as to whether or not the protect switch S6 is located at the releasing position (REMOVE) for releasing the protect, and if it is located at the
20 releasing position, the releasing data is outputted, the protect display is turned OFF (steps P422 to P424), and the sequence returns to step P401. If the switch S4 is not located at the releasing position, the sequence immediately returns to the step P401.

If the judgment at step P420 shows that the data is not protected,
25 a judgment is made as to whether or not the protect switch S6 is located

in ON position, and if it is in ON position, a predetermined value K2 is set to the timer 1, thereby starting to count time (steps P425 to P427). The judgment at step P426 shows that the switch S6 is not located in ON position, the sequence returns to step P401. A judgment is made as to whether or not the protect/erase operation switch S6 is turned ON during the time counting process of the timer 1 (step P428), and if it is ON, the protect data is outputted to the IC card or the inner memory through the data bus DB2 so as to be written therein, the protect display is turned ON, and after the switch S6 has been turned OFF (steps P429 to P432), the sequence returns to step P401.

Here, in the above-mentioned preferred embodiment, the period at which the protect switch S6 is operated is regulated by the time K2 that has been set in the timer 1, and only when the switch S6 is operated during this period, the protect operation is executed; however, in addition to this arrangement, for example, the setting period of the protect may be set to a period during which images are switched to the next one.

With respect to the judgment at step P402, an explanation will be given of the single-frame erasing mode. In these processes, the processes of steps P441 to P455 (Fig. 13(c)) are the same as those processes of steps P403 to P417 at the time of the reproducing mode (Figs. 13(a)(b)), the explanation thereof is omitted.

At step P456, the protect data of the image to be reproduced is read out. A judgment is made as to whether or not there is protect data applied to the image to be reproduced, and if there is no protect data, that is, the data is not protected, the image signals are outputted, and if the

protect data is recorded, the sequence proceeds to step S443 so as to process the next frame (steps P457 to P458). The above-mentioned processes make it possible to prevent the image to be protected from being reproduced, and thereby from being erroneously erased.

5 A judgment is made as to whether or not the protect/erase operation switch S7 is turned ON (step P459), and if this is ON, the erasing data is outputted to the signal processing CPU 51, and after the erasing process of the recorded image has been completed, the erase display is turned ON (steps P459 to P462). Then, after the switch S7 has
10 been turned OFF, the sequence proceeds to step P401. In the case when the judgment at step P459 shows that the switch S7 is not ON, the sequence also proceeds to step P401.

 Figs. 14(a) to 14(d) are flow charts that show processes, such as a back-feeding process of image frames at the time of reproducing the
15 recorded images and a back-feeding process of image frames at the time of erasing images frame by frame, carried out by the operations of the access switch S5 (DOWN) that is shown as step P113 of the flow chart shown in Fig. 7. First, a judgment is made as to whether or not the mode switching switch S3 is set to the reproducing mode (PLAY) (step P501),
20 and if it is not the reproducing mode, a judgment is made as to whether or not the erasing mode frame by frame is (S-ERASE) ON, and if it is the erasing mode, the sequence proceeds to step P541, and if it is not the erasing mode, the sequence returns to the main routine (step P502).

 When the judgment at step P501 shows the reproducing mode, a
25 judgment is made as to whether or not the access switch S5 is switched

from OFF to ON (step P503, P504), and each time the switching is made from OFF to ON, the contents of the counter are decremented by 1 (step P505), and a judgment is made as to whether or not any IC card 41 has been inserted (step P506). If it has been inserted, a judgment is made as to whether or not the contents of the counter have become 0 (step P507). If the contents of the counter are 0, this indicates that all the frames recorded in the IC card 41 have been reproduced; therefore, the counter is set to 10 so that the inner memory mode is set so as to reproduce the images recorded in the inner memory 40 (step P508, P509). If the judgment at step P507 shows that the contents of the counter are not 0, a judgment is made as to whether or not the inner memory mode is set, and if the inner memory mode is set, a judgment is made as to whether or not the contents of the counter are 0 (step P510, P511). In the case when the contents of the counter are 0, this indicates that all the frames recorded in the inner memory 40 have been reproduced; therefore, the counter is set to 32, and the IC card mode is set so as to reproduce images recorded in the IC card 41 (step P512, P513). If the judgment at step P510 or P511 is negative, the sequence proceeds to step P516. Moreover, if the judgment at step P506 shows that no IC card is inserted, a judgment is made as to whether or not the contents of the counter are 0, and if the contents of the counter are 0, the counter is set to 10, and if not 0, the sequence immediately proceeds to step P516 (step P514, P515).

Processes of steps P516 to P532 including the process for outputting image signals from the image recording frames and the process for recording and releasing the protect data by the operation of

the protect/erase operation switch S6 are the same as those of steps P416 to P432 in the processes of the access switch S4; therefore, the explanation thereof will be omitted.

An explanation will be given of a process in the case of the single-frame erasing mode indicated by the judgment of the step P502. The process, which starts with step P541, includes steps P541 to P555 (Fig. 14(c)) that have the same contents of the process as those of the steps P503 to P517 (Figs. 14(a)(b)) in the case of the reproducing mode. Moreover, the processes of steps P556 to P563 (Fig. 14(d)), which are the single-frame erasing processes, have the same contents of the processes as those processes indicated by steps P456 to P463 (Fig. 13(d)) of the process by the access switch S4. Therefore, the explanation thereof is omitted.

Figs. 15(a) to 15(c) are flow charts that show processes indicating the automatic frame-forwarding (AUTO) process at the time of image reproducing that is selected by the frame-forwarding switching switch S8, which is indicated as step P115 in the flow chart shown in Fig. 7.

When the automatic frame-forwarding process is selected by the operation of the switch S8, a judgment is first made as to whether or not the function switching switch S3 is in the image reproducing mode (PLAY) or in the erasing mode (S-ERASE) frame by frame (step P601, P602), and only in the case of these two modes, the sequence proceeds to step P603 and thereafter.

A judgment is made as to whether or not the access switch S4 is switched from OFF to ON, and if it is not switched in this manner, the

same judgment is made on the access switch S5 (step P603, P604). In the case when the switch S4 is switched from OFF to ON, a predetermined value K4 is set to the timer 4, thereby starting to count time, and the contents of the counter are incremented by 1 (steps P605 to
5 P607).

In steps P608 to P621, depending on the fact that all the frames recorded in the IC card have been reproduced or that all the frames recorded in the inner memory have been reproduced, the inner memory mode or the IC card mode is set, and the images are reproduced, and the
10 images are reproduced so that the image signals are outputted; and these steps are the same as the steps P406 to P418 in the processes of the access switch S4. Therefore, the explanation thereof is omitted here.

A judgment is made as to whether or not the access switch S4 or S5 has been switched from OFF to ON (steps P622 to P624) prior to the
15 completion of the time counting process of the timer 4 (steps P622 to P624). If the time counting process of the timer 4 has been completed first, the sequence returns to step P605, and a time counting process is again started out by the timer 4 so as to carry out the reproducing process on the next image. Moreover, when the switch S4 or the switch S5 is
20 turned ON prior to the completion of the time counting process of the timer 4, the time counting process of the timer 4 is stopped so as to read the protect data of the reproducing images (step P625, P626).

In steps P626 to P639, the protect data of the reproducing images is read out, and the recording and releasing of the protect data are carried
25 out by the operation of the protect/erase operation switch S6; and since

these steps are the same as the aforementioned steps P419 to P432 in the processes of the access switch S4. Therefore, the description thereof is omitted here.

5 In the case when the judgment at step P604 shows that the access switch S5 has been switched from OFF to ON, the sequence proceeds to step P641. First, a predetermined value K4 is set to the timer 4, thereby starting to count time, and the contents of the counter are decremented by 1 (steps P641 to P643).

10 In steps P644 to P657, depending on the fact that all the frames recorded in the IC card have been reproduced or that all the frames recorded in the inner memory have been reproduced, the inner memory mode or the IC card mode is set, and the images are reproduced so that the resulting image signals are outputted; and these steps are the same as the aforementioned steps P506 to P518 of the processes by the access
15 switch S5. Therefore, the description thereof is omitted here.

A judgment is made as to whether or not the access switch S4 or S5 has been switched from OFF to ON prior to the completion of the time counting process of the timer 4 (steps P658 to P660). In the case when the time counting process of the timer 4 has been completed first, the
20 sequence returns to step P641, and a time counting process is again started by the timer 4 so as to reproduce the next image. Moreover, in the case when the switch S4 or S5 has been turned ON prior to the completion of the time counting of the timer 4, the sequence proceeds to step P625, thereby carrying out the recording and releasing processes of
25 the protect data in the same manner as described earlier.

Fig. 16 is a flow chart that shows the manual frame-forwarding process (MANUAL) at the time of reproducing images that is selected by the frame-forwarding switching switch S8 shown as step P117 in the flow chart of Fig. 7. As clearly shown by this flow chart, when the switch S8 is set to MANUAL, each time the access switch S4 is switched from OFF to ON, the aforementioned process of S4 is executed, and each time the access switch S5 is switched from OFF to ON, the aforementioned process of S5 is executed.

Fig. 17 is a flow chart that shows the date setting process shown as step P119 in the flow chart shown in Fig. 7. First, when the date setting switch S13 is turned ON, the "year" setting mode is started, and the access switches S4 and S5 are operated so as to set a desired year (step P701). When the mode shift switch S12 is turned ON, the modes are switched to the "month" setting mode, and the access switches S4 and S5 are operated so as to set a desired month (step P702, P703).

Thereafter, in the same manner, the mode shift switch S12 and the access switches S4 and S5 are operated so as to set "date", "hour" and "minute" are set (steps P704 to P709). A judgment is made as to whether or not the date setting switch S13 is turned ON (step P710), and if it is not ON, the sequence returns to step P701, and the date setting process is again provided. If it is ON, the date setting process is completed so that the sequence returns to the main routine. The display on the right side of Fig. 17 shows one example of the display state of the display section 13 in the respective steps.

Here, in the present preferred embodiment, after the completion

of the setting of “minute”, the state of the switch S13 is judged; however, the state of the switch S13 may be judged after the data setting of each mode, and in the case of ON, the display may be set to the original state.

Figs. 18(a) and (b) are flow charts that indicate the process for
5 transferring images recorded in the inner memory to the IC card, when
the IC card is inserted. First, a judgment is made as to whether or not
any IC card 41 has been inserted to the camera (step P801), and if it has
been inserted, the signal CSDP is allowed to go “Low” so that the memory
state of the IC card is sent from the signal processing CPU 51, and the
10 signal CSDP is allowed to go “High”, thereby completing the
communication (steps P802 to P804). A judgment is made as to whether
the IC card is unrecorded or the inner memory has any recorded images
(step P805, P806), and if the IC card is unrecorded and there is any
recorded image in the inner memory, the sequence proceeds to step P807.
15 If the IC card has been recorded or the inner memory has no recorded
images, the sequence returns to the main routine.

Supposing that the leading frame number of the recorded images
in the inner memory is X (in this preferred embodiment, 10), and that the
leading frame number of the recordable areas in the IC card is Y (in this
20 preferred embodiment, 32) (step P807, P808), modes are switched to the
inner memory mode, and the contents of the counter are set to X so that
image data is read from the frame of the inner memory corresponding to
the contents of the counter X, and stored in the buffer memory (steps
P809 to P812). In the present preferred embodiment, this process is
25 controlled by the signal processing CPU 51 so that after the completion of

the process (step P813), the contents of the counter X are again outputted, thereby erasing the image data in the corresponding frame in the inner memory (steps P814 to P815). After completion of the erasing process (step P816), the IC card mode is set, and the contents of the counter are
5 set to Y so that the image data, stored in the buffer memory, is recorded in the frame of the IC card corresponding to the contents of the counter Y (steps P817 to P820). After completion of the recording process (step P821), the inner memory mode is again set so that the frame number X of the inner memory to be processed is decremented by 1, thereby preparing
10 for the processing of the next frame (steps P822 to P823). A judgment is made as to whether or not the frame number is 0, and if it is not 0, this indicates that there are frames to be processed so that a new frame number X is set to the counter, and the image data is read from the frame of the inner memory corresponding to the contents of the counter X, and
15 stored in the buffer memory (steps P824 to P827). After completion of the process (step P828), the contents of the counter X is again outputted and the image data of the corresponding frame in the inner memory is erased (steps P829 to P830). After the completion of the erasing process (step P831), the IC card mode is set, and the contents of the counter Y is
20 decremented by 1 so that the image data, stored in the buffer memory, is recorded in the frame in the IC card corresponding to the new contents of the counter Y; thus, after the completion of the process (step P832 to P837), the sequence returns to step P822 so as to process the next frame.

When the judgment at step P824 shows $X = 0$, that is, when all the
25 image data recorded in the inner memory have been processed, the

number of recordable frames in the IC card is subtracted by the number of frames stored in the inner memory, and a display is provided so as to indicate that the IC card is recordable from this frame number, thereby completing the processes (steps P840 to P841).

5 Here, in the above-mentioned preferred embodiments, the IC card to which images recorded in the inner memory are transferred is limited to an unrecorded card; however, an IC card in which image data is partially recorded may be used so as to record data in the partially unrecorded areas. Moreover, in the above-mentioned preferred
10 embodiment, images in all the frames stored in the inner memory are transferred to the IC card; however, only the images in protected frames may be transferred.

Fig. 19 shows a display example of the display section 5. Among display elements of the display section 5, 5a is a display element that
15 represents a frame number of each image that is processed in various modes such as recording, protective, reproducing and erasing operations, 5b is a display element that indicates the insertion of the IC card, 5c is a display element that shows a mode (year, month, data, time) at the time of the date setting process. Moreover, 5d is a display element indicating
20 the protective mode, 5e is a display element indicating the reproducing mode, and 5f is a display element indicating the single-frame erasing mode.

Figs. 19(a), (b) and (c) are display examples that show the recording mode; and 19(a) indicates that an IC card is inserted and the IC
25 card is set so that 32 frames of images can be recorded therein. Fig.

19(b) indicates by slanting lines in the center of the display 5b that all the frames in the IC card have been recorded, while 10 frames of images can be recorded in the inner memory. Fig. 19(c) indicates that no IC card is inserted, while the inner memory is set so that 10 frames of images can be recorded.

Figs. 19(d), (e) and (f) show display examples in the case of the protective mode, and Figs. 19(g), (h) and (i) show display examples in the case of the reproducing mode, while Figs. 19(j), (k) and (l) indicate the single-frame erasing mode in which "S-ERASE" is displayed. In the case when of the all-frame erasing mode, "A-ERASE" is displayed.

In the above-mentioned preferred embodiment, the IC card is used as a recording medium for recording digital image signals; however, instead of this, a magnetic disk may be used so as to record analog image signal.

[Effects of the Invention]

As described above, in accordance with the present invention, an image recorded in a first image recording medium installed in a camera is transferred and recorded in a second image recording medium that is freely detachably attached to the camera; therefore, upon reproducing images, it is not necessary to connect the camera to a reproducing apparatus, and the IC card is directly inserted to the reproducing apparatus, thereby making it possible to greatly improve the operability.

4. Brief Description of the Drawing

Fig. 1 is a perspective view that shows the external appearance of

a camera in accordance with the present invention, Fig. 2 is a block diagram that shows a control circuit of the camera, Fig. 3 is a block diagram that shows a signal processing section in the control circuit in detail, Fig. 4 is a perspective view that shows the external appearance of a flash device, Fig. 5 is a circuit diagram of the flash device, Fig. 6 is a perspective view that shows the construction of an image pickup section, Figs. 7 to 17 are flow charts that explain the control operations of the camera, in which Fig. 7 is a flow chart that shows the outline of the entire controlling operation, Fig. 8 is a flow chart that shows a process in which a mode switching switch is OFF, Fig. 9 is a flow chart that shows a process in a recording mode, Fig. 10 is a flow chart that shows a process in which a switch S1, which is activated by pressing a release button to the first stage, is turned ON, Fig. 11 is a flow chart that shows a process in a reproducing mode, Fig. 12 is a flow chart that shows a process in an erasing mode, Fig. 13 is a flow chart that shows a process in which an access switch S4 is used, Fig. 14 is a flow chart that shows a process in which an access switch S5 is used, Fig. 15 is a flow chart that shows an automatic frame-forwarding process by a frame-forwarding switch S8, Fig. 16 is a flow chart that shows a manual frame-forwarding process by a frame-forwarding switch S8, and Fig. 17 is a flow chart that shows a date setting process by a date setting switch S13; Fig. 18 is a flow chart that shows a process for transferring recorded images in an inner memory to an IC card to be recorded therein, and Fig. 19 is a drawing that shows a display example of a display section.

1: camera main body, 2: pickup lens, 4: release button, 5: display

section, 7: macro pickup light-projection window, 8: IC card insertion slot,
9: flash device connecting section, S3: mode switching switch, S4, S5:
access switch, S6: protect switch, S7: protect/erasing operation switch,
S8: frame-forwarding switching switch, S9: macro pickup switch, S10:
5 flash pickup switch, 30: CPU, 31: signal processing section, 40: inner
memory, 41: IC card.



Fig. 2

- 36 PHOTOMETER CIRCUIT
- 35 CLOCK GENERATION CIRCUIT
- 37 FLASH DEVICE
- 5 31 SIGNAL PROCESSING SECTION
- 41 IC CARD
- 40 INNER MEMORY
- 38 POWER SUPPLY
- 5 DISPLAY
- 10

Fig. 3

- 55 BUFFER MEMORY
- 53 ADDRESS GENERATION CIRCUIT
- 52 SIGNAL PROCESSING CIRCUIT
- 15 51 SIGNAL PROCESSING CPU
- 41 IC CARD
- 40 INNER MEMORY

Fig. 7

- 20 開始 START
- P101 OFF PROCESS
- P102 RECORDING MODE
- P103 RECORDING MODE PROCESS
- P105 S1 ON PROCESS
- 25 P106 REPRODUCING MODE

P107 REPRODUCING MODE PROCESS

P108 ERASING MODE

P109 ERASING MODE PROCESS

P111 S4 PROCESS

5 P113 S5 PROCESS

P115 AUTOMATIC FORWARDING PROCESS

P117 MANUAL FORWARDING PROCESS

P119 DATE SETTING PROCESS

終了 END

10

Fig. 8

OFF 処理 OFF PROCESS

P131 PORT-TIMER RESET

P132 PROTECT DISPLAY ON?

15 P133 PROTECT DISPLAY OFF

P134 COMPLETION DISPLAY ON?

P135 COMPLETION DISPLAY OFF

P136 IC CARD DISPLAY ON?

20 P137 IC CARD DISPLAY OFF

P138 DATE DISPLAY OFF

P139 COUNTER DISPLAY OFF

P140 PWC → H

リターン RETURN

25

Fig. 9

記録モード処理 RECORDING MODE PROCESS

P153 IC CARD ON?
P154 IC CARD DISPLAY ON
5 P156 CARD DATA INPUT
P158 IC CARD UNRECORDABLE ?
P160 COMPLETION DISPLAY ON
P161 COUNTER DISPLAY ON
P162 DATE SETTING DISPLAY ON
10 リターン RETURN
P166 INNER MEMORY DATA INPUT
P171 PLAY DISPLAY OFF

Fig. 10(a)

15 リターン RETURN
P207 FLICKERING DISPLAY
S1 ON 処理 S1 ON PROCESS
P201 RECORDING MODE?
P202 COUNTER = 0 ?
20 P203 TIMER 1 START COUNTING
P204 COUNTER FLICKERING DISPLAY
P205 TIMER 1 COMPLETED?
P206 COUNTER LIGHT UP
リターン RETURN
25 P210 MACRO PICKUP S9 ON?

P211 LAMP LA → ON
 P212 INPUT PHOTOMETER VALUE
 P213 MACRO PICKUP S8 ON?
 P214 COUNTER LIGHT ?
 5 P215 LOW LUMINANCE ?
 P216 FLASH S11 ON?

Fig. 10 (b)

P230 FLASH MODE?
 10 P231 COUNTER LIGHT
 P239 LAMP LA → OFF
 リターン RETURN

Fig. 10(c)

15 P240 SHUTTER PL → ON
 P241 START EXPOSING
 P243 MACRO PICKUP S9 ON?
 P247 FLASH MODE
 P248 TIMER 2 → 2·TV_C
 20 P249 TIMER 2 START
 P250 TIMER 2 COMPLETION?
 P251 TIMER 2 → 2·TV_F
 P252 TIMER 2 START
 P253 TIMER 3 → LIGHT EMISSION TIMING
 25 P254 TIMER 3 START

P255 TIMER 2 COMPLETION?
P256 TIMER 3 COMPLETION?
P257 FLASH LIGHT EMISSION
P258 STOP LIGHT EMISSION

5

Fig. 10(d)

P260 SHUTTER PL OFF
P262 MACRO PICKUP S9 ON?
P263 FLASH S11 ON?
10 P264 LAMP LA OFF
P259 WRITE ADDITIONAL DATA

Fig. 10(e)

P273 TIMER 1 \leftarrow K2
15 P274 TIMER 1 START TIME COUNTING
P276 WRITE PROTECT DATA
P277 PROTECT DISPLAY ON

P272 PROTECT DISPLAY OFF
20 P279 TIMER 1 COMPLETION?

Fig. 10(f)

P280 COUNTER \leftarrow (n - 1)
P281 COUNTER n = 0 ?
25 P282 IC CARD ON?

P283 COUNTER \leftarrow 10
 P284 DISPLAY COMPLETION ON
 P285 SET INNER MEMORY MODE
 P286 READ INNER MEMORY
 5 P287 INPUT PROTECT DATA
 P288 PROTECT DATA?
 P289 S1 OFF?
 P291 TIMER 1 \leftarrow K1
 P292 PROTECT FLICKERING DISPLAY
 10 P293 TIMER 1 COMPLETION?
 P294 PROTECT DISPLAY ON
 P295 PROTECT DISPLAY OFF
 P296 COUNTER DISPLAY ON
 リターン RETURN

15

Fig. 11

再生モード処理 REPRODUCING MODE PROCESS

P302 PLAY DISPLAY ON
 P303 CSDP \rightarrow L
 20 P304 PLAY MODE
 P308 IC CARD ON?
 P309 CARD DISPLAY ON
 P311 COUNTER \leftarrow "32"
 P312 SET CARD MODE
 25 P317 COUNTER \rightarrow ADB1

P318 COUNTER DISPLAY
 P307 ERASE DISPLAY OFF
 P313 CARD DISPLAY OFF
 P315 COUNTER ← “10”
 5 P316 SET INNER MEMORY MODE
 P319 IMAGE SIGNAL OUTPUT
 S4 処理 S4 PROCESS
 S5 処理 S5 PROCESS
 P322 ANOTHER MODE?
 10 リターン RETURN

Fig. 12(a)

消去モード処理 ERASING MODE PROCESS
 P333 PLAY DISPLAY OFF
 15 P335 “A” DISPLAY OFF
 P336 “S” DISPLAY ON
 P338 S-ERASE MODE
 P340 IC CARD ON?
 P341 CARD DISPLAY ON
 20 P343 COUNTER ← “32”
 P344 SET CARD MODE
 P345 CARD DISPLAY OFF
 P347 COUNTER ← “10”
 P348 SET INNER MEMORY MODE

Fig. 12 (b)

P350 COUNTER \rightarrow ADB1

P351 COUNTER DISPLAY

P352 READ PROTECT DATA

5 P353 PROTECT DATA?

P354 OUTPUT IMAGE SIGNAL

P357 OUTPUT ERASING DATA

P359 ERASE DISPLAY ON

P355 COUNTER $\leftarrow (n - 1)$

10 S4 処理 S4 PROCESS

S5 処理 S5 PROCESS

P363 ANOTHER MODE?

リターン RETURN

15 Fig. 12(c)

P371 "S" DISPLAY OFF

P372 "A" DISPLAY ON

P374 A-ERASE MODE

P377 OUTPUT ERASING DATA

20 P379 FLICKERING ERASE DISPLAY

P381 ERASE DISPLAY ON

P382 IC CARD ON?

P383 COUNTER \leftarrow "32"

P384 COUNTER \leftarrow "10"

25 P385 COUNTER DISPLAY ON

リターン RETURN

Fig. 13(a)

S4 処理 S4 PROCESS

5 P401 REPRODUCING MODE?
P402 SINGLE-FRAME ERASING MODE?
P405 COUNTER $\leftarrow (n + 1)$
P406 IC CARD ON?
P407 COUNTER = 33?
10 P408 COUNTER \leftarrow "1"
P409 SET INNER MEMORY MODE
P410 INNER MEMORY MODE?
P411 COUNTER = 11?
P412 COUNTER \leftarrow "1"
15 P413 SET IC CARD MODE
リターン RETURN
P414 COUNTER = 11?
P415 COUNTER \leftarrow "1"

20 Fig. 13(b)

P416 COUNTER \rightarrow ADB1
P417 COUNTER DISPLAY
P418 OUTPUT IMAGE SIGNAL
P419 READ PROTECT DATA
25 P420 PROTECT DATA?

P421 PROTECT DISPLAY ON
 P422 S6 RELEASING POSITION ?
 P423 OUTPUT RELEASING DATA
 P424 PROTECT DISPLAY OFF
 5 P425 S6 ON POSITION?
 P426 TIMER 1 \leftarrow K2
 P427 TIMER 1 START COUNTING TIME
 P428 S6 ON POSITION?
 P429 OUTPUT PROTECT DATA
 10 P430 PROTECT DISPLAY ON
 P431 S6 OFF POSITION?
 P432 TIMER 1 COMPLETION?

Fig. 13(c)

15 P443 COUNTER \leftarrow (n + 1)
 リターン RETURN
 P444 IC CARD ON?
 P445 COUNTER = 33?
 P446 COUNTER \leftarrow 1
 20 P447 SET INNER MEMORY MODE
 P448 INNER MEMORY MODE?
 P449 COUNTER = 11?
 P450 COUNTER \leftarrow 1
 P451 SET IC CARD MODE
 25 P452 COUNTER = 11?

P453 COUNTER \leftarrow 1
P454 COUNTER \rightarrow ADB1
P455 COUNTER DISPLAY

5 Fig. 13(d)

P456 READ PROTECT DATA
P457 PROTECT DATA?
P458 OUTPUT IMAGE SIGNAL
P460 OUTPUT ERASING DATA

10 P462 ERASE DISPLAY ON?

Fig. 14(a)

S5 処理 S5 PROCESS

P501 REPRODUCING MODE?

15 P502 SINGLE-FRAME ERASING MODE?

リターン RETURN

P505 COUNTER \rightarrow (n - 1)

P506 IC CARD ON?

P507 COUNTER = 0?

20 P508 COUNTER \rightarrow 10

P509 SET INNER MEMORY MODE

P510 INNER MEMORY MODE?

P511 COUNTER = 0?

P512 COUNTER \leftarrow 32

25 P513 SET IC CARD MODE

P514 COUNTER = 0
P515 COUNTER ← 10

Fig. 14 (b)

5 P516 COUNTER → ADB1
P517 COUNTER DISPLAY
P518 OUTPUT IMAGE SIGNAL
P519 READ PROTECT DATA
P520 PROTECT DATA
10 P521 PROTECT DISPLAY ON
P522 S6 RELEASING POSITION
P523 OUTPUT RELEASING DATA
P524 PROTECT DISPLAY OFF
P525 S6 ON POSITION?
15 P526 TIMER 1 ← K2
P527 TIMER 1 START COUNTING TIME
P529 OUTPUT PROTECT DATA
P530 PROTECT DISPLAY ON
P532 TIMER 1 COMPLETION
20

Fig. 14(c)

リターン RETURN
543 COUNTER ← (n - 1)
P544 IC CARD ON?
25 P545 COUNTER = 0?

P546 COUNTER \leftarrow 10
 P547 SET INNER MEMORY MODE
 P548 INNER MEMORY MODE?
 P549 COUNTER = 0?
 5 P550 COUNTER \leftarrow 32
 P551 SET IC CARD MODE
 P552 COUNTER = 0?
 P553 COUNTER \leftarrow 10
 P554 COUNTER \rightarrow ADB1
 10 P555 COUNTER DISPLAY

Fig. 14(d)

P556 READ PROTECT DATA
 P557 PROTECT DATA
 15 P558 OUTPUT IMAGE SIGNAL
 P560 OUTPUT ERASING DATA
 P562 ERASE DISPLAY ON

Fig. 15(a)

20 P601 PLAY MODE?
 P605 TIMER 4 \leftarrow K4
 P606 TIMER 4 START COUNTING TIME
 P607 COUNTER \leftarrow (n + 1)
 P608 IC CARD ON?
 25 P609 COUNTER = 33?

P610 COUNTER \leftarrow 1
 P611 SET INNER MEMORY MODE
 P612 INNER MEMORY MODE?
 P613 SET IC CARD MODE
 5 リターン RETURN
 P602 SINGLE-FRAME ERASING?
 P617 COUNTER = 11?
 P618 COUNTER \leftarrow 1
 P614 COUNTER = 11?
 10 P615 COUNTER \leftarrow 1
 P616 SET IC CARD MODE

Fig. 15(b)

P619 COUNTER \rightarrow ADB1
 15 P620 COUNTER DISPLAY
 P621 OUTPUT IMAGE SIGNAL
 P624 TIMER 4 COMPLETION?
 P625 TIMER 4 STOP
 P626 READ PROTECT DATA
 20 P627 PROTECT DATA?
 P628 PROTECT DISPLAY ON
 P629 S6 RELEASING POSITION
 P630 OUTPUT RELEASING DATA
 P631 PROTECT DISPLAY OFF
 25 P632 S6 ON POSITION

P633 TIMER 1 \leftarrow K2
 P634 TIMER 1 START TIME COUNTING
 P636 OUTPUT PROTECT DATA
 P637 PROTECT DISPLAY ON
 5 P639 TIMER 1 COMPLETION?

Fig. 15(c)

P641 TIMER 4 \leftarrow K4
 P642 TIMER 4 START COUNTING TIME
 10 P643 COUNTER \leftarrow (n - 1)
 P644 IC CARD ON?
 P645 COUNTER = 0 ?
 P646 COUNTER \leftarrow 10
 P647 SET INNER MEMORY MODE
 15 P648 INNER MEMORY MODE?
 P649 SET IC CARD MODE
 P653 COUNTER = 0
 P654 COUNTER \leftarrow 10
 P650 COUNTER = 0?
 20 P651 COUNTER \leftarrow 32
 P652 SET IC CARD MODE
 P655 OUTPUT COUNTER CONTENTS
 P656 COUNTER DISPLAY
 P657 OUTPUT IMAGE SIGNAL
 25 P660 TIMER 4 COMPLETION?

Fig. 16

手動駒送り処理 MANUAL FRAME-FORWARDING PROCESS

S4 処理 S4 PROCESS

5 S5 処理 S5 PROCESS

リターン RETURN

Fig. 17

S13 ON 処理 S13 ON PROCESS

10 P701 SET YEAR (S4, S5, ON)

P702 SHIFT MODE (S12 ON)

P703 SET MONTH

P704 MODE SHIFT

P705 SET DATE

15 P706 MODE SHIFT

P707 SET TIME

P708 MODE SHIFT

P709 SET MINUTE

リターン RETURN

20

Fig. 18(a)

IC カード記録処理 IC CARD RECORDING PROCESS

P801 IC CARD ON?

P803 INPUT CARD DATA

25 P805 IC CARD UNRECORDED?

P806 INNER MEMORY RECORDING EXIST?

P807 LEADING FRAME No. X OF THE RECORDED IMAGE IN THE
INNER MEMORY

P808 LEADING FRAME No. Y OF THE RECORDABLE AREA IN THE

5 IC CARD

P809 SET INNER MEMORY MODE

P810 COUNTER \leftarrow X

P811 OUTPUT COUNTER CONTENTS

P812 STORE CONTENTS OF INNER MEMORY IN B-MEMORY

10

Fig. 18(b)

P822 SET INNER MEMORY MODE

P825 COUNTER \leftarrow X

P826 OUTPUT COUNTER CONTENTS

15 P827 INNER MEMORY \rightarrow B-MEMORY

P829 OUTPUT COUNTER CONTENTS

P830 OUTPUT ERASING DATA

P840 32 INNER MEMORY NUMBER OF RECORDED FRAMES

P841 DISPLAY COUNTER

20 リターン RETURN

P832 SET IC CARD MODE

P834 COUNTER \leftarrow Y

P835 OUTPUT COUNTER CONTENTS

P836 B-MEMORY \rightarrow MEMORY IC CARD

25

Fig. 19

記録モード RECORDING MODE

プロテクトモード PROTECTIVE MODE

再生モード REPRODUCTIVE MODE

5 消去モード ERASING MODE

IC カード IC CARD

IC カード（記録終了） IC CARD (RECORDING END)

内部メモリ INNER MEMORY